DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark A. Wilson (Reg. # 43,994) on Monday 6/15/2009.

2. The application has been amended as follows:

In the Claims

In claim 1, line 4:

replace "which" with - - the active structures and the additional filling structure - -.

In claim 10, line 5:

replace "which" with - - the active structures and the additional filling structure - -.

(This Examiner's Amendment has been made in order to place the application into a condition for allowance).

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

Claims 1-6 and 8-14 are allowed because the prior art made of record does not teach or suggest a security-sensitive semiconductor product in the manner as recited in the claims.

4. With respect to claims 1-6 and 8-14, the prior art fails to teach the combination of steps in claims 1 and 10 including the following particular steps as recited in claims 1 and 10:

wherein the parts of the filling structures that are generated are combined with the contacts so that additional circuit functions are generated in addition to the electrically active circuit structures that are produced for the circuit;

wherein a majority of the fill structures generated are incorporated along a signal path so that active, electrically connected parts of the fill structures are situated next to dummy fill structures that are insulated from the electrically active structures and the active electrically connected parts of the fill structures

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suchin Parihar/
Examiner, Art Unit 2825

/Jack Chiang/

Supervisory Patent Examiner, Art Unit 2825